REMARKS

Reconsideration and allowance are respectfully requested. Claims 23-31 and 33-44 remain pending.

Claims Indicated as Allowable

Preliminarily, Applicant thanks the Examiner for the indication that claims 27-31 are allowed (upon submission of a terminal disclaimer), and claims 38-44 would be allowable if rewritten in independent form.

Terminal Disclaimer

A terminal disclaimer is submitted herewith to overcome the obviousness-type double-patenting rejection of claims 23-31 and 33-44.

Objection to Abstract

The abstract is objected to for being lengthy and containing legal phraseology. A replacement abstract on a separate sheet is submitted herewith that is believed to overcome the objection.

Claim Rejections

Claims 23-26 and 33-37 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,250,569 to Sasaki, et al. ("Sasaki"). Claims 23-26 and 33-37 are also rejected under 35 U.S.C. § 102(b) as being anticipated by JP Pub. 5-86864 to Koichi ("Koichi"). Claims 23-26 and 33-37 are additionally rejected under 35 U.S.C. § 102(b) as being anticipated by JP Pub. 5-87027 to Hiroshi, et al. ("Hiroshi"). Applicant respectfully traverses these rejections for the following reasons.

Independent claim 23 recites that a transistor has a first data state and a second data state. The first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in a semiconductor layer. The second data state is a state in which a forward

bias is applied between the semiconductor layer and a drain diffusion region to extract the excessive majority carriers from within the semiconductor layer to the drain diffusion region.

The Office Action alleges that Sasaki discloses a first data state written by impact ionization and a second data state written through a forward bias. To the contrary, Sasaki does not use a forward bias as in claim 23. In Sasaki, a "0" bit is written by a charge pumping operation (col. 5, line 51 to col. 6, line 12). As clearly shown in Fig. 2B, the pumping operations between a positive voltage and zero voltage are applied to gate G (address line AD1) several times, such that the holes and electrons in the semiconductor layer (body) are recombined and the holes and electrons in the semiconductor layer are eliminated. The physical principle of the charge pumping action is different from that of claim 23, in which a forward bias is applied between the semiconductor layer and the drain diffusion region to extract the excessive majority carriers. That is, Sasaki does not apply the forward bias between the semiconductor layer and the drain diffusion region in the second data state, as claimed.

Regarding Koichi, Figs. 2(a) and 2(b) illustrate how to write "0" data and "1" data in a memory cell. As shown in Fig. 2(a), for writing "1" data, 5V is applied to both the gate and the drain, and then the gate voltage is reduced to 0V before the drain voltage is reduced to 0V. When the gate voltage is reduced to 0V, the state in which the holes are generated by impact ionization is held in the body.

As further shown in Fig. 2(b) of Koichi, when writing "0" data, 5V is applied to both the gate and the drain. The drain voltage is then reduced to 0V before the gate voltage is likewise reduced. When the gate voltage is reduced to 0V, the state in which in which holes are not generated by impact ionization is held in the body.

Therefore, in Koichi, a difference between writing "0" data and writing "1" data is whether or not the impact ionization is generated when the gate voltage is reduced to 0V. In addition, forward bias is not applied when writing "0" data. In other words, the "0" data state is

the reference state, and the impact ionization is generated to increase the holes in the body. That is, a forward bias is not applied as claimed to write "0" data.

Referring to Hiroshi, Figs. 2(a) and 2(b) illustrate how to write "0" data and "1" data in a memory cell. Similar to Koichi, the difference between writing "0" and "1" data is whether or not the impact ionization is generated when the gate voltage is reduced to 0V. Again, a forward bias is not applied as claimed when writing "0" data.

As further shown in Fig. 2(b) of Hiroshi, when writing "1" data, 5V is applied to both the gate and the drain to generate the impact ionization. The gate voltage is then reduced to 0V before the drain voltage is likewise reduced. When the gate voltage is reduced to 0V, the state in which holes are generated by impact ionization is held in the body.

As shown in Fig. 2(a) of Hiroshi, when writing "0" data, 5V is applied to the gate and 2.5V is applied to the drain, to avoid generating impact ionization. The gate voltage is then reduced to 0V before the drain voltage is likewise reduced. When the gate voltage is reduced to 0V, the state in which holes are not generated by impact ionization is held in the body. Therefore, the memory cell of Hiroshi does not use a forward bias as claimed.

For at least these reasons, it is submitted that claim 23 distinguishes over the three asserted references and is therefore allowable.

It is submitted that independent claim 35 is also allowable for at least similar reasons as described above with regard to claim 23.

It is further submitted that the dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

All objections rejections having been addressed, it is believed that the present application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions or feel that an interview would be desirable, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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Dated: February 7, 2007